



**THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re application of

U-MING KO

Serial No. 10/743,079 (TI-29632.1)

Filed December 23, 2003

For: INPUT/OUTPUT ARCHITECTURE FOR INTEGRATED CIRCUIT

Art Unit 2891

Examiner Steven J. Fulk

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JMC

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences

STATUS OF CLAIMS

This is an appeal of claims 42, 45, 48 and 51, all of the rejected claims. Claims 43, 44, 46, 47, 49, 50, 52 and 53 have been allowed and claims 1 to 41 have been cancelled and are the subject of the parent application which is now Patent No. 6,376,352. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 42 relates to a semiconductor wafer which includes a plurality of integrated circuits (as shown in Figs. 4 and 5 and specification at page 6, line 11 to end of page), each integrated circuit separated from the other integrated circuits by a scribe region (120, 122) at the periphery of each integrated circuit. Each integrated circuit includes a centrally disposed core region (40), at least one bond pad (112) disposed between the core region and the scribe region, an electrostatic discharge device (114, page 8, last line) and an I/O buffer (116) disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region.

Claim 45 relates to an integrated circuit which includes a semiconductor substrate which includes (as shown in Figs. 4 and 5 and specification a page 6, line 11 to end of page) a scribe at the periphery of the substrate (120, 122) and a centrally disposed core region (40), at least one bond pad (112) disposed between the core region and the scribe region, an electrostatic discharge device (114) and an I/O buffer (116) dispensed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region.

Claim 48 relates to a method of fabricating a semiconductor wafer which includes (as shown in Figs. 4 and 5 and specification at page 6, line 11 to end of page) the steps of providing a plurality of integrated circuits, each integrated circuit separated from the other integrated circuits by a scribe region at the periphery of each integrated circuit. Each integrated circuit is provided with a centrally disposed core region (40), at least one

bond pad (112) disposed between the core region and scribe region, an electrostatic discharge device (114) and an I/O buffer (116) disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region.

Claim 51 relates to a method of fabricating an integrated circuit which includes (as shown in Figs. 4 and 5 and specification at page 6, line 11 to end of page) the steps of providing a semiconductor substrate which includes a scribe (120, 122) at the periphery of the substrate and a centrally disposed core region (40). At least one bond pad (112) is disposed between the core region and the scribe region. An electrostatic discharge device (114) and an I/O buffer (116) is disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 42, 45, 48 and 51 are anticipated under 35 U.S.C. 102(a) by Applicant's Admitted Prior Art (AAPA).

ARGUMENT

To begin with, the rejection is based upon 35 U.S.C. 102(a). The requirement for such a rejection, even were the examiner's allegation as to the content of AAPA to be correct, which it is not, defies the requirements of the statute. A rejection using this section of the statute requires that structure or method step and its function as claimed be found in a single reference. The examiner admits that this is not the case by stating, according to the examiner's interpretation of AAPA, that AAPA must be altered (turned 90°) to achieve the result that the examiner alleges.

Furthermore, claim 42 requires, among other features, “an I/O buffer disposed between said scribe region and said core region and *laterally* of said bond pad relative to said core region and said scribe region” (underline and italics not in original). No such structure is taught or even remotely suggested by AAPA.

The allegation that figure 3 can be turned 90 degrees in the clockwise direction to achieve that which is claimed is without merit.

To begin with, there is no teaching or even a remote suggestion to turn Fig. 3 by 90 degrees. There would also be no reason to turn Fig. 3 by 90 degrees. Furthermore, if Fig. 3 is turned 90 degrees the above noted feature is still not found. This argument also applies to all of the claims discussed hereinbelow wherein this feature is claimed, namely claims 45, 48 and 51. If Fig. 3 of the subject specification is turned by 90°, the I/O buffer 16 is still directly between the bond pad and the core and scribe region and not laterally of the bond pad relative to the core and scribe regions. The I/O buffer is directly in line with all of the other claimed elements. The term “lateral” means –on the side--. The rejected claims require that the I/O buffer not only be on the side of (laterally) the bond pad, but also on the side of the bond pad relative to the core and scribe regions. This feature is specifically claimed, found in Figs. 4 and 5 of the subject disclosure and not found in any of the figures of the subject application listed as being “PRIOR ART” or AAPA. Note that in each of Figs. 1 and 3 that the I/O buffer (16), the ESP (14) and the bond pad (12) are in a direct line between the core (40) and the scribe lines (20, 22).

Claim 45 requires, among other features, “an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core

region and said scribe region". No such structure is taught of suggested by AAPA either alone or in the combination as claimed for the reasons stated above.

Claim 48 requires, among other features, "an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region". No such structure is taught of suggested by AAPA either alone or in the combination as claimed for the reasons stated above.

Claim 51 requires, among other features , "providing an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region". No such step is taught of suggested by AAPA either alone or in the combination as claimed for the reasons stated above.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



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CLAIMS APPENDIX

The claims on appeal read as follows:

42. A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

45. An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

46. An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad;

and

an I/O buffer disposed between said scribe region and said core region.

48. A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

51. A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing a electrostatic discharge device; and

providing an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

EVIDENCE APPENDIX

N/A

RELATED PROCEEDINGS APPENDIX

N/A